REMARKS

Claims 24-47 remain in this application. Claims 1, 3-10, 12-20, 22, and 23 have been cancelled without prejudice. These claims have not been cancelled in order to overcome any cited art of which Applicants are aware but rather to rewrite the claims in an alternate form for greater ease of understanding. Claims 24-47 have been added. The Applicants respectfully request reconsideration of this application in view of the above amendments and the following remarks.

35 U.S.C. §103(a) Rejection - Wasson

The Examiner has previously rejected former claims 1, 3-10, 12-20, and 22-23 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,181,151 B1, issued to Wasson (hereinafter referred to as "Wasson"). These claims have been cancelled. The Applicants respectfully submit that the present claims are allowable over Wasson.

Claim 24 recites an integrated circuit comprising "*a test controller; a logic unit controller of the integrated circuit; a single test bus of the integrated circuit, the single test bus coupled between the test controller and the logic unit controller; a plurality of design for test features of the integrated circuit, the design for test features coupled to the logic unit controller; and a logic unit of the integrated circuit, the logic unit coupled to the logic unit controller and to the design for test features, wherein the test controller is to provide a global control signal as a packet including a plurality of different types of instruction signals to the logic unit controller over the single test bus, wherein the logic unit controller is to receive the packet and provide a plurality of different types of instruction signals to a design for test feature*".

Applicants respectfully submit that Wasson does not teach or reasonably suggest these limitations. In particular, Wasson does not teach or reasonably suggest either: (1)

an integrated circuit including the claimed test controller, the logic unit controller, the single test bus, the plurality of design for test features, and the logic unit; or (2) a test controller to provide a global control signal as a packet including different types of instruction signals over a single test bus, and the logic unit controller to receive the packet and to provide different types of instruction signals to a design for test feature.

Firstly, Wasson does not teach or suggest an integrated circuit including the claimed test controller, the logic unit controller, the single test bus, the plurality of design for test features, and the logic unit. FIG. 1 of Wasson shows an integrated circuit (IC) tester 10 (see e.g., column 3, lines 54-55). Among other components, the IC tester 10 includes a IC device under test (DUT) 14, tester channels CH(1)-CH(N), a host computer 16, a system disk drive 17, a disk controller 18, and a disk drive 20 (see e.g., FIG. 1 and column 4, lines 31-33). As clearly shown, the host computer, the system disk drive, the disk controller, and the disk drive, are external to, and are not integrated with, the DUT. Furthermore, it is clearly explained that the tester channels CH(1)-CH(N) each carry out test activities at a separate terminal or pin of the DUT during a test (see e.g., column 3, lines 56-58, and pin electronics circuit 40 of FIG. 2). Pins are used to connect integrated circuits to external devices. Accordingly, the tester channels, disk drive, etc. are not part of an integrated circuit, as is clearly claimed in claim 1. For at least this reason, claim 1 is believed to be allowable.

The Examiner has argued that even if the tester is external to the device under test, it would be an obvious engineering design choice to integrate the tester with the device under test, since built-in self testing is well known in the art of testing integrated circuits. Applicants respectfully submit that the modification of Wasson proposed by the Examiner is inappropriate. Wasson does not teach or reasonably suggest that the tester channels CH(1)-CH(N), disk controller, or like external components, may be integrated with the DUT. That is, there is simply is no suggestion or motivation to modify the

reference in the manner proposed by the Examiner. Furthermore, modifications that are not taught or suggested in the prior art would be needed in order to modify Wasson in the manner proposed by the Examiner. There is no guarantee that the modification proposed by the Examiner would even be operative or desirable. That is, there is no reasonable expectation of success.

Applicants respectfully remind the Examiner that in order to establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). For at least the reasons, the modification of Wasson proposed by the examiner is believed to be inappropriate. Accordingly, the Examiner has not established a prima facie case of obviousness.

Secondly, even if Wasson is modified as proposed by the Examiner, the modified Wasson still does not teach or suggest all the claim limitations. In particular, there still is no teaching or suggestion of a test controller to provide a global control signal as a packet including different types of instruction signals over a single test bus, and the logic unit controller to receive the packet and to provide different types of instruction signals to a design for test feature. As Applicants have previously argued, and the Examiner has conceded, Wasson does not teach, suggest, or even mention that a packet is transmitted in the DUT for purposes of testing. Furthermore, there is absolutely no teaching or suggestion in Wasson of a packet that includes different types of instruction signals and

that may be transmitted over a single test bus. For at least these reasons, the Examiner has not established a prima facie case of obviousness.

For the Examiner's convenience, Applicants would like to point out sections of the patent application that may help the Examiner to understand the aforementioned limitation of claim 24. As discussed in the present patent application, one global test control line may conventionally be run between the test controller 252 and a DFT feature for each type of instruction signal (see e.g., page 9, lines 8-10). As further discussed in the patent application, the corresponding large number of lines may tend to limit arrangement of lines, take up space, and affect timing of signals distributed on the lines (see e.g., page 9, lines 20-28). Alternatively, a test controller may provide a global control signal as a packet including a plurality of different types of instruction signals to a logic unit controller over a single test bus, and the logic unit controller may receive the packet and provide a plurality of different types of instruction signals to a design for test feature, as claimed in claim 24.

Accordingly claim 24, and its dependent claims, are believed to be allowable. Independent claims 37 and 44, and their respective dependent claims, are also believed to be allowable for one or more reasons similar to those discussed above for claim 24.

Conclusion

In view of the foregoing, it is believed that all claims now pending patentably define the subject invention over the prior art of record and are in condition for allowance. Applicants respectfully request that the rejections be withdrawn and the claims be allowed at the earliest possible date.

Request For Telephone Interview

The Examiner is invited to call Brent E. Vecchia at (303) 740-1980 if there remains any issue with allowance of the case.

Request For An Extension Of Time

The Applicants respectfully petition for a two-month extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a). Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17 for such an extension.

Charge Our Deposit Account

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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